27. (Amended) A data storage medium storing instructions which, when executed by a computer system, cause the computer system to perform a method comprising:

identifying partial feasible routing solutions corresponding to each of a subset of a set of wires to be routed, each of the partial feasible routing solutions identifying a feasible route between points fixed in a layout;

merging the partial feasible routing solutions to identify one or more feasible routing solutions for the set of wires to be routed.

*REMARKS*

Reconsideration of the present application is respectfully requested. Claims 1-30 previously presented for examination remain in the application. Claims 1, 9, 13, 20, 22 and 27 have been amended to place the claims in better form for consideration on appeal.

The drawings filed on December 20, 1999 were deemed to be acceptable subject to correction of informalities indicated on the "Notice of Draftsperson's Patent Drawing Review," PTO-948 (paper #13), however, correction is stated to be required in order to avoid abandonment of this application. Applicants have submitted formal drawings concurrently herewith.

Claims 1-30 stand rejected under 35 U.S.C. § 102(e) as being considered to be anticipated by U.S. Patent No. 5,987,086 to Raman et al. ("Raman").

Claim 1 includes the limitations

identifying partial feasible routing solutions corresponding to each of a subset of a set of wires to be routed, each of the partial feasible routing solutions identifying a feasible route between fixed points;

merging the partial feasible routing solutions to identify one or more feasible routing solutions for the set of wires to be routed.

(Claim 1)(emphasis added).

Applicants respectfully submit that Raman fails to teach or suggest the claimed features of applicants' invention including at least identifying partial feasible routing solutions for each of a subset of a set of wires to be routed and then merging the partial feasible routing solutions to identify one or more feasible routing solutions for a set of wires to be routed.

As previously discussed, Raman discloses an approach geared towards interconnecting transistors and other devices in order to optimize the area of a layout cell while honoring performance constraints. (Raman, Abstract).

In accordance with Raman, routing is performed in a series of passes including a pre-routing step, remaining nets are routed using an area-based router, an initial coarse routing is performed, and a determination is made whether the routing is acceptable. If not, the routing space is expanded and routing costs and via costs are modified to improve the solution.

In contrast, claim 1 sets forth identifying partial feasible routing solutions for a subset of a set of wires to be routed, and then merging the partial feasible routing solutions for each of the subsets to identify one or more feasible routing solutions for the set of wires to be routed. By identifying partial feasible routing solutions for each subset of a set of wires to be routed and then merging them to

identify one or more feasible routing solutions as set forth in claim 1, it may be possible to avoid ripping up already routed wires and re-routing them as in Raman.

It is stated in the Office Action that the local routing solutions set forth in column 25 of Raman teach the claimed partial feasible routing solutions.

Applicants respectfully submit that the local routing solutions discussed at claim 25 cannot be considered to teach the claimed partial feasible routing solutions that are merged to identify feasible routing solutions. The local routing solutions set forth at claim 25 are not merged to identify feasible routing solutions, but rather are used to identify the cost of moving a layout object through a move operation (see e.g. col. 24, lines 30-34). There is no teaching or suggestion in Raman of merging the described local routing solutions to identify a feasible routing solutions for all of the identified wires.

It is further stated in the Office Action that Figs. 28-29 describe the claimed partial feasible routing solutions. Figure 28 sets forth Raman's approach for multi-layered detailed routing. Figure 29 sets forth Raman's approach for pre-routing as part of that approach. As clearly described in Raman at, for example, col. 35, line 64 and col. 36, lines 66-67, Raman uses a sequential routing approach in which one net is routed and then another net is routed. There is no teaching or description in Raman of determining the partial feasible routing solutions for a first set of wires, merging the partial feasible routing solutions for the first set of wires with the partial feasible routing solutions for a second set of wires and identifying a routing solution for the union of the first and

second sets by merging the partial feasible routing solutions for the first and second sets of wires. Using a sequential routing approach, there is no merging of partial feasible routing solutions to identify a feasible routing solution as set forth in the claims.

For at least the above reasons, Raman cannot be considered to teach or suggest the claimed features of applicants' invention.

Independent claims 9, 15, 20, 22 and 27 each include limitations similar to those argued above in reference to claim 1. Claims 2-8, claims 10-14, claims 16-19, claim 21, claims 23-26 and claims 28-30 depend from and limit claims 1, 9, 15, 20, 22 and 27, respectively. Thus, claims 2-30 are also patentably distinguished over Raman for at least the same reasons.

Raman also does not teach or suggest providing a routing tree as set forth in claims 9, 15 and 25.

It is suggested in the Office Action that Raman teaches the claimed routing tree in, for example, Figs. 40-42. Figure 40 is a flow chart illustrating the operation of the Minimize Wire Length function, Figure 41 is a flow chart illustrating the Find Local Slack function, and Figure 42 is a flow chart illustrating the operation of the Calculate On-Grid Slack routine, each of which is related to the compaction process. These trees are not used to merge partial feasible routing solutions as set forth in the claims, but rather to assess the impact of moving layout objects that are represented by vertices to determine the layout that will result in minimum wire length. (see e.g. Raman, col. 43, lines 42 - 64 and col. 44, lines 6-55). While different routes may result from moving the layout

objects, the tree set forth in Raman does not identify multiple feasible routing solutions between fixed points in a layout as set forth in the claims.

Applicants respectfully submit that the applicable objections and rejections have been overcome and claims 1-30 are in condition for allowance. If the examiner disagrees or believes that further discussion will expedite prosecution of this case, he is invited to telephone applicants' representative at the number indicated below.

If there are any charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

Dated: 4/14, 2003

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new issue

and not in spec.

## VERSION OF AMENDED CLAIMS WITH MARKINGS TO SHOW CHANGES

1. (Amended) A method comprising:

identifying partial feasible routing solutions corresponding to each of a subset of a set of wires to be routed, each of the partial feasible routing solutions identifying a feasible route between fixed points in a layout; not in spec

merging the partial feasible routing solutions to identify one or more feasible routing solutions for the set of wires to be routed.

9. (Amended) A method comprising:

constructing multiple partial feasible routing trees, each of the partial feasible routing trees identifying a set of partial feasible routing solutions for a subset of a set of wires to be routed, each of the partial feasible routing solutions identifying feasible routes between fixed points in a layout; and

merging the multiple partial feasible routing trees to identify a set of feasible routing solutions for the set of wires to be routed.

15. (Amended) A method comprising:

determining a first set of possible routes between a first set of fixed points in an integrated circuit layout;

determining a second set of possible routes between a second set of fixed points in the integrated circuit layout;

merging the first and second sets of possible routes to determine a third set of possible routes, the third set of possible routes including possible routes from the first and second sets of possible routes that do not conflict.

20. (Amended) An apparatus comprising:

an integrated circuit device having wires routed according to a method comprising:

identifying partial feasible routing solutions corresponding to each of a subset of a set of wires to be routed, each of the partial feasible routing solutions identifying a feasible route between two nodes fixed in layout;

merging the partial feasible routing solutions to identify one or more feasible routing solutions for the wires to be routed; and

selecting the routing solution of one or more feasible routing solutions.

22. (Amended) A data storage medium storing instructions to be executed by a computer system, the instructions comprising:

a maze router to determine partial feasible routing solutions [between] for each of a subset of a set of wires to be routed, each of the partial feasible routing solutions to identify a feasible route between fixed points in a layout; and

a deferred merging router to merge the partial feasible routing solutions to generate one or more feasible routing solutions.

27. (Amended) A data storage medium storing instructions which, when executed by a computer system, cause the computer system to perform a method comprising:

identifying partial feasible routing solutions corresponding to each of a subset of a set of wires to be routed, each of the partial feasible routing solutions identifying a feasible route between points fixed in a layout;

merging the partial feasible routing solutions to identify one or more feasible routing solutions for the set of wires to be routed.